

Clock Programmable Mixer for Fuze IF with Filter

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Presented at the 56th Annual
Fuze Conference in Baltimore,
Maryland on May 16, 2012

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**Mixed Signal
Integration**

This presentation is on the MSMXVHF integrated circuit. This standard product from MSI includes a mixer and filter, and has potential uses for an IF section in electronic fuzes.

Mixed Signal Integration is a Silicon Valley chip maker specializing in analog and mixed-signal CMOS based integrated circuits. Founded in 1997, MSI offers both standard products and custom ASICs. MSI enjoys excellent customer relationships in markets such as consumer, wireless communications, automatic test equipment and the defense industry. MSI is a member of NWECC, the National Weapons and Energetics Consortium. To date, MSI has designed custom ASICs for three DOTC initiatives.

The chip we will be discussing today was originally designed as a standard product for commercial applications. It was NOT designed for a DOTC initiative.

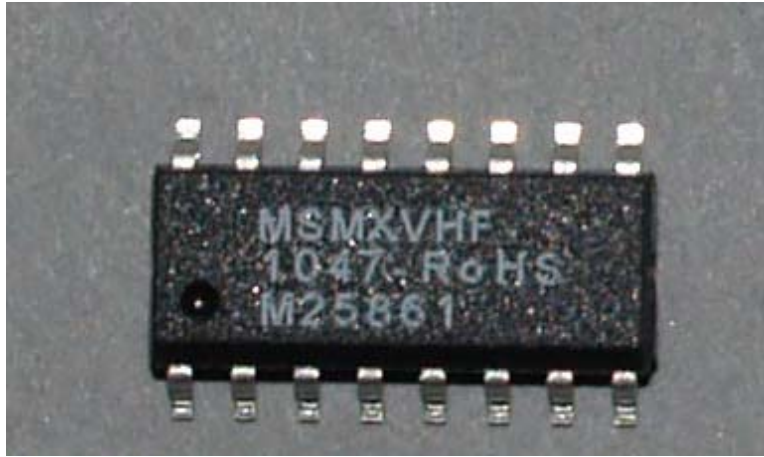
MSMXVHF

- 600 MHz Differential Switching Mixer
 - Simple CMOS Design
 - ~6 dB loss
 - Differential analog input for common mode rejection
- Switched-Capacitor Lowpass/Bandpass Filter
 - Clock programmable
 - Selectable Gain



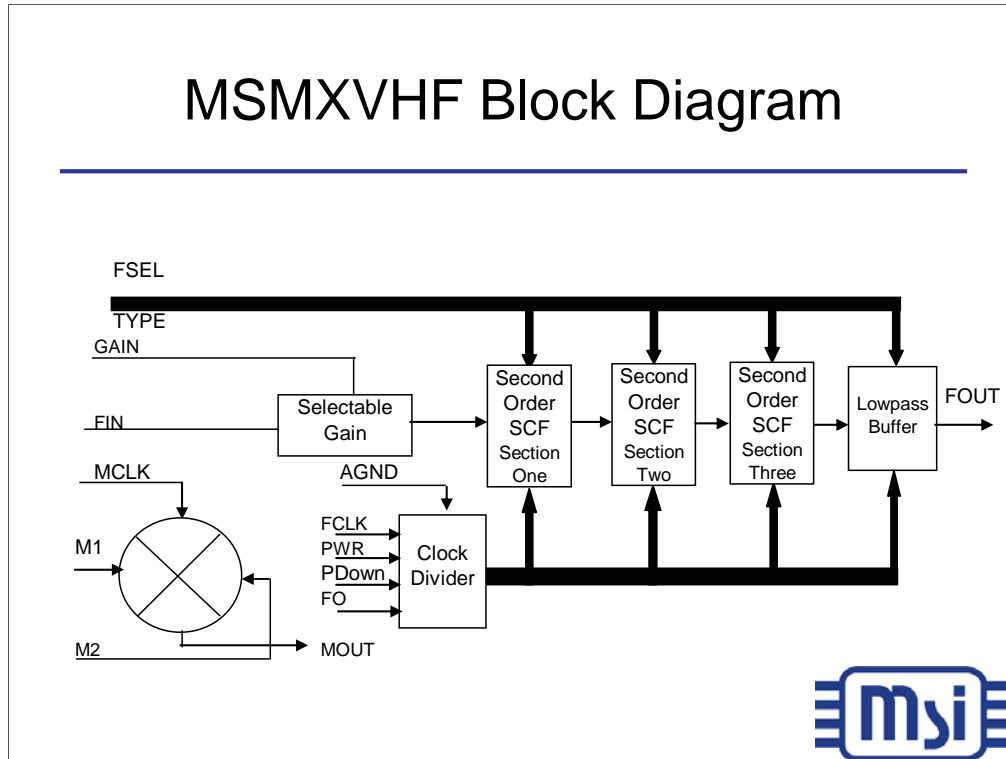
The MSMXVHF Mixer with selectable high frequency lowpass/bandpass filter IC is a CMOS chip that has an independent mixer for IF functions. The output of the mixer can be tied to an internal filter, which is pin selectable to either lowpass or a band-pass shape. The lowpass response can be a 6 pole Butterworth, Elliptic or Bessel filter. The band pass response can be a six pole full, 1/3 or 1/6 octave bandpass filter. The device uses switched-capacitor filters and no external components (except for decoupling capacitors) are required. Two external clocks are needed for the mixer and filter functions. A low current mode is pin selectable. This option works at lower frequencies.

MSMXVHF



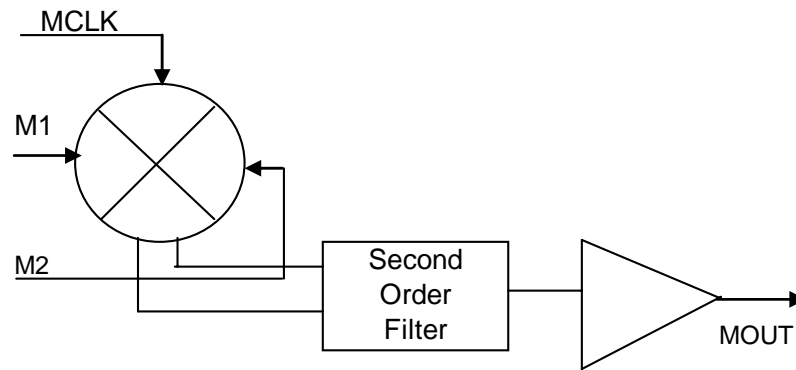
Here is a photograph of the MSMXVHF. The device is available in a SOIC-16 150 mil narrow package (39 mm square excluding leads) and a VQFN-28 4x4mm (16 mm square) in the future. Although these parts are packaged in Lead-free RoHS plastic and leadframes, we can supply in more traditional Tin/Lead lead finish.

MSMXVHF Block Diagram



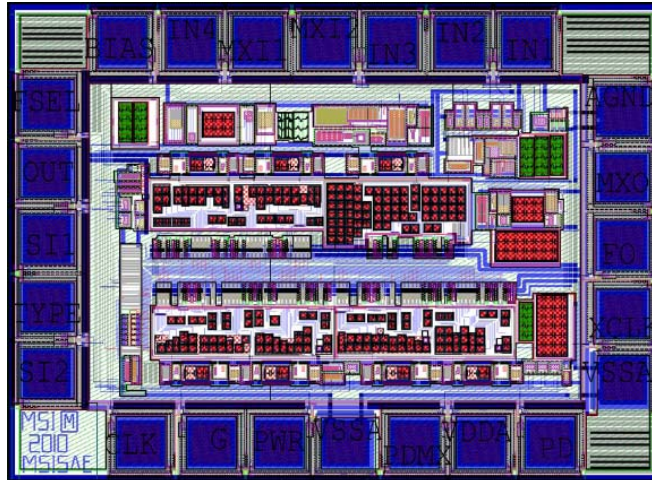
This is the block diagram of the MSMXVHF. The mixed-signal mixer is independent of the filter section. Two synchronized clocks of different frequencies can be used to separate the mixer local oscillator from the filter clock, which sets the filter center frequency (for bandpass) or corner frequency (for lowpass).

MSMXVHF Mixer Detail



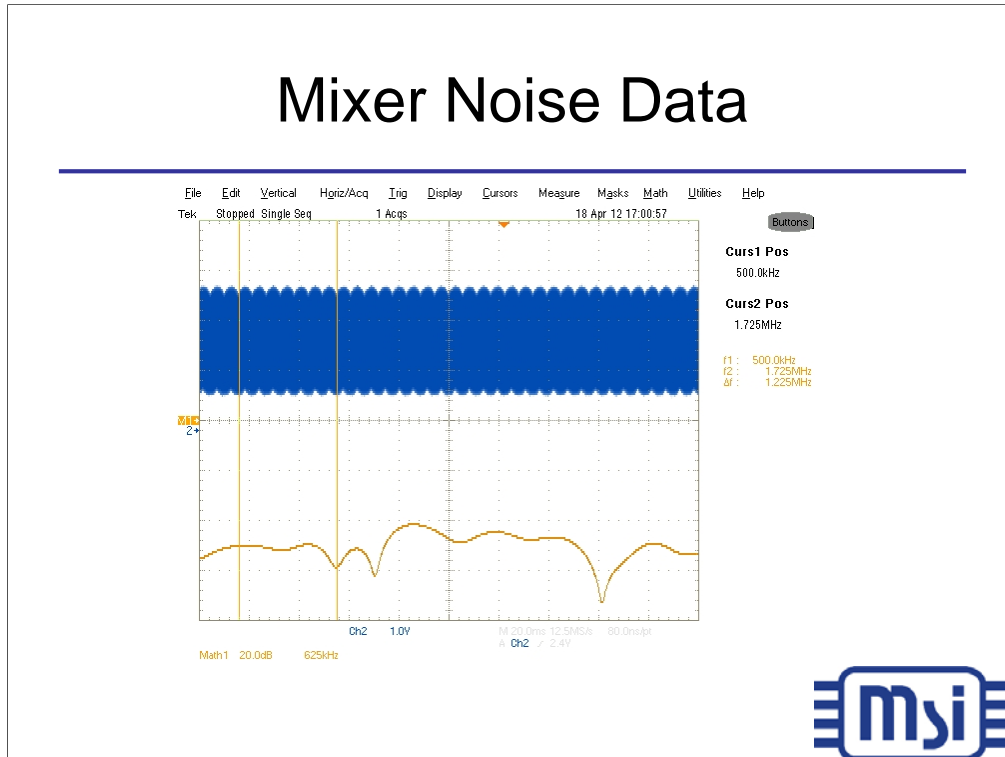
The mixer of the MSMXVHF provides a continuous time second order lowpass filter set at approximately 1 MHz. Since the maximum switched capacitor filter center/corner frequency is up to 1 MHz, this filter reduces any local oscillator clock (MCLK) feedthrough.

MSMXVHF Die Detail



This is a plot of the device layout of the MSMXVHF. The design is in 0.35um double-Polysilicon, double-metal CMOS. The die is small enough to easily fit into a 28 leadless VQFN 4x4mm package.

Mixer Noise Data



The noise data is taken with a 15 MHz LO and the mixer clock inputs grounded. The top trace of the scope display shows the mixer clock input in the time domain. The bottom trace of the display shows the output of the mixer in the frequency domain. The mixer output has been observed as low as -80 dB.

The top trace shows the mixer clock input at about 3 V_{p-p}. {Point laser}

The first cursor line for the bottom trace is at 500 kHz. {Point laser}

The second cursor line for the bottom trace is at about 1.7 MHz. (Point laster)

MSMXVHF Evaluation Board



This photograph is of the MSMXVHF evaluation board. The board provides BNC inputs for the differential input signal, mixer clock, and filter clock. The Filter Output is a test point to reduce external capacitance of a BNC connector. The socket at the upper left is for an on-board crystal oscillator, to be used instead of an external mixer clock. The dual inline pin (DIP) pads in the center of the board are for a socket to easily change parts for evaluation.

System Issues

- Clocks must be synchronized.
- Frequency output of mixer $< 1\text{MHz}$.
- Subsequent stages must be in sync.

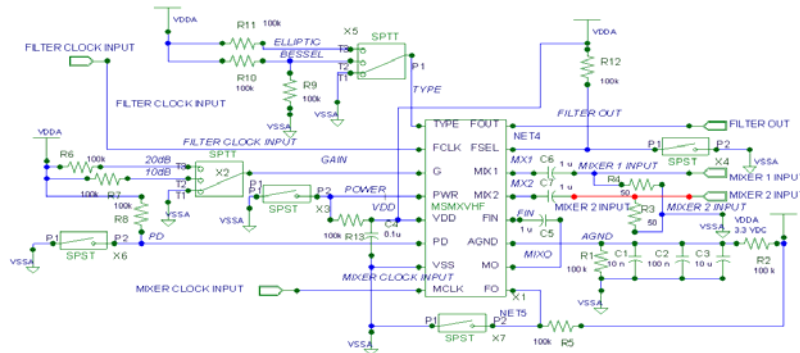


In order to reduce random clock noise, the mixer clock and the filter clock must be in sync. This does not mean that they need to be the same frequency. A synchronized filter clock, either by divider or PLL, will provide the synchronization needed.

Next, the difference between the mixer clock and the analog mixer input must be less than 1 MHz, or the second order continuous-time lowpass filter will attenuate the output.

Finally, the clock for the stages that follow the MSMXVHF must be in sync as well, to prevent an increase in noise.

Simplified Application Schematic



The simplified schematic shows the connections of the MSMXVHF with signals and clocks. FOUT is the filtered output from the mixer/filter combination. The switches for filter type, lowpass or bandpass, power, powerdown, and clock-to-corner ratio are CMOS levels.

Technical Issues

- Maximum mixer input 500 MHz
- Filter limit is 1 MHz lowpass or bandpass
- Mixer output is limited to < 1MHz
- Device maximum VDD is 3.3VDC



The mixer input operates up to 500 MHz. The switched-capacitor filter of the MSMXVHF can be adjusted from DC up to 1 MHz. The mixer output is also limited to slightly below 1 MHz output. The maximum DC for the MSMXVHF is 3.3V, the output of some Lithium battery cells. A new design in a smaller geometry, such as a 0.18 μm process would achieve higher mixer and filter frequencies.

Summary

The MSMXVHF integrated circuit:

- Mixing up to 500 MHz.
- Filtering to 1 MHz
- Operation at up to 3.3V



In future designs, in smaller geometries, the maximum mixing frequency may be increased to above 1 GHz. The technology described here could be integrated into more complex integrated circuits.