06/2023

Selectable High Frequency LP/BP Filter Data Sheet

MSHFS1/MSHFS2/MSHFS3/MSHFS4/MSHFS5/MSHFS6

Description

The selectable high frequency lowpass/ bandpass filter IC Is a CMOS chip that can be configured for either a lowpass or a band-pass filter. The lowpass response can be a 6 pole Butterworth, Elliptic or Bessel filter. The band pass response can be a six pole full, third or sixth octave bandpass filter. The device uses switched-capacitor filters and no external components (except for decoupling capacitors) are required, Only an external clock is needed.

A four input multiplexor and externally select-able gain setting pin, along with a power down and clock to corner ratio select pin are in-cluded in the 16 pin version. An 8 pin version is also available for compact PC board lay-outs. MSHFS3, MSHFS4 and MSHFS6 are lower current, lower frequency versions.

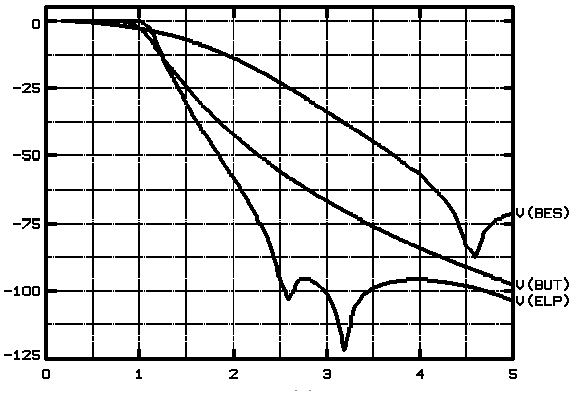
Features

Six Filter Types In One Package
No External Components
Switched-Capacitor Filters
High Frequency Operation
Input Multiplexor
Adjustable Gain 0, 10 or 20 dB
Small Package Size
Low Cost
On Chip Power Save Pin
ANSI Compatible Bandpass

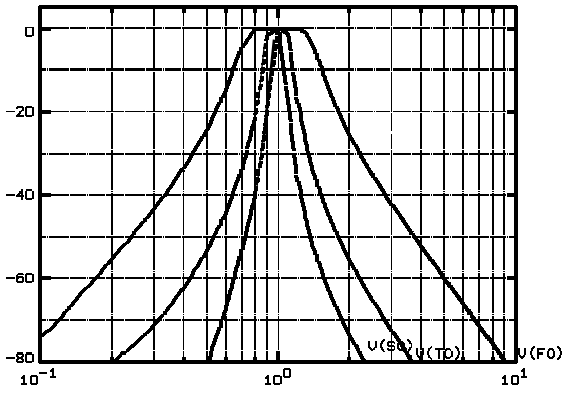
Applications

Spectrum Analyzers
General Purpose Systems
Portable Systems
Anti-Alias Filters
Reconstruction Filters
Telecommunications
Tracking Filters
Harmonic Analysis
Noise Analysis
Data Communication
Wireless Applications

Lowpass Responses



Bandpass Responses



Electrical Characteristics

(VDD = +5.0V, T = 20° C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Specifications						
Operating Voltage	VDD		4.0	5.0	5.5	V
Supply Current	IDD	MSHFS1, MSHFS2, MSHFS5		24	30	mA
Supply Current	IDD	MSHFS3, MSHFS4, MSHFS6		4	9	mA
Supply Current in Power Down Mode	IDD			200		uA
AC Specifications						
Gain	Av		-0.5	0	0.5	dB
Noise	en	To 1/2 Sample		350		uVrms
Distortion	THD	A weighted		-61		dB
Signal Swing		1 kHz	3.5	4.0		V p-p
Input Impedance	ZIN			1.0		Mohm
Output Drive	Io			400		uA
Output Impedance	Zo			500		ohm
Output Capacitive Load					20	pF
Clock to Corner		MSHFS5, MSHFS6		12.5		
Clock to Corner		MSHFS1, MSHFS3		6.25		
Clock to Corner		MSHFS2, MSHFS4, Fo=1		12.5		
Clock to Corner		MSHFS2, MSHFS4, Fo=0		6.25		
Center Frequency Range	Fo	MSHFS1, MSHFS2, MSHFS5	0.00001	3		MHz
Center Frequency Range	Fo	MSHFS3, MSHFS4, MSHFS6	0.00001	1		MHz
Ripple						
Elliptic Lowpass				0.2		dB
Full Octave				0.2		dB
Third Octave				0.2		dB
Sixth Octave				0.2		dB
Stop Band Rejection						
Elliptic Lowpass				70		dB
Bessel Lowpass				60		dB
40 dB Bandwidth						
Full Octave		Normalized Fo	0.3		3	
Third Octave		Normalized Fo	0.6		1.67	
Sixth Octave		Normalized Fo	0.76		1.32	
Bandpass Q						
Full Octave Q	Q			1.5		
Third Octave	Q			4.5		
Sixth Octave	Q			9		

note 1: Sample rate ratio is 2X clock to corner ratio.

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Filter Selection

The filter type is selected using the two filter select pins, TYPE and FSEL, FSEL is a CMOS level pin that selects lowpass or bandpass (lowpass = 0, bandpass = 1). TYPE Is a tertiary control pin that selects the filter response. State 0 is VSS, state 1 is GND and state 2 is VDD.

TYPE	Lowpass	Bandpass
0	Butterworth	Full Octave
1	Bessel	Third Octave
2	Elliptic	Sixth Octave

Pin Description

1. TYPE — Filter Response Select Pin.
2. S2 — Input Multiplexor Select Pin
3. CLK — Sine Wave Clock Input CMOS Level
4. G — Gain Select Pin
5. VDD — Positive Power Supply,Typically 2.5 Volts for Split Supply, 5.0 Volts for Single Supply
6. PD — Power Down Pin, CMOS level, Hi = Power Down
7. VSS — Negative Power Supply, Typically 2.5 Volts for Split Supply, 0 Volts for Single Supply
8. F0 — Clock to Corner Select Pin
9. GND — GND Pin, OV for Split Supplies 2.5 Volts Typical for Single Supply
10. IN1 — Input 1, Select Code 00
11. IN2 — Input 2, Select Code 01
12. IN3 — Input 3, Select Code 10
13. IN4 — Input 4, Select Code 11
14. FSEL — Selects Filter O = Low Pass, 1 = Bandpass
15. Out — Filter Output
16. S1 — Input Multiplexor Select Pin

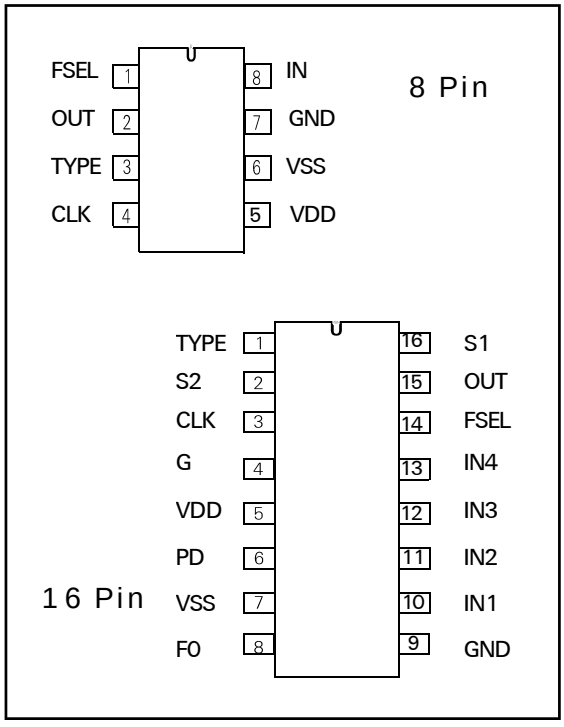
Gain and Frequency Selection

The Gain control pin G is a tertiary control pin where state 0 is VSS, state 1 is GND level and state 2 is VDD.

G	Gain
0	OdB
1	10dB
2	20dB

The frequency control pin F0 is a CMOS level pin where HIGH is clock to corner of 12.5 to 1 (25 to 1 for Bessel) and LOW is clock to corner of 6.25 to 1 (12.5 to 1 for Bessel). The sample rate ratio is twice the clock to corner ratio (double sampling).

Pin Configuration



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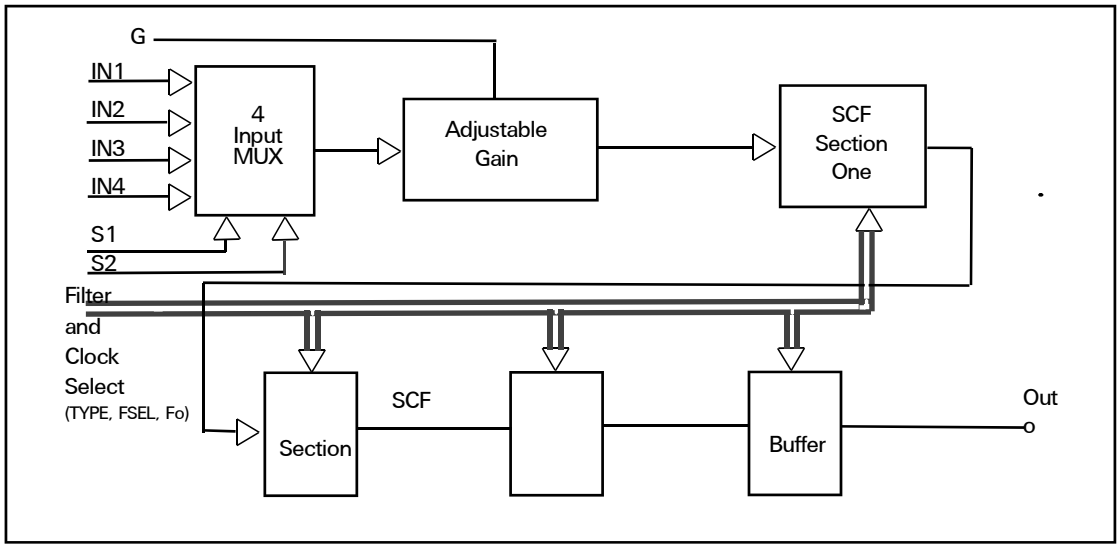
Block Diagram



Absolute Maximum Ratings

Power Supply Voltage	+6V
Storage Temperature	-60 to +150 C
Operating Temperature	-40 to +85 C

Part Number	Package	Operating Temperature
MSHFS1P	8 Pin Dip	-40 - +85 C
MSHFS2P	16 Pin Dip	-40 - +85 C
MSHFS3P	8 Pin Dip	-40 - +85 C
MSHFS4P	16 Pin Dip	-40 - +85 C
MSHFS5P	8 Pin Dip	-40 - +85 C
MSHFS6P	8 Pin Dip	-40 - +85 C
MSHFS1N	8 Pin SOIC	-40 - +85 C
MSHFS2S	16 Pin SOIC	-40 - +85 C
MSHFS3S	8 Pin SOIC	-40 - +85 C
MSHFS4S	16 Pin SOIC	-40 - +85 C
MSHFS5S	8 Pin SOIC	-40 - +85 C
MSHFS6S	8 Pin SOIC	-40 - +85 C

Add "TR" suffix to part number (ie. MSHFS1NTR) for Tape & Reel.
Add "TR-RoHS" suffix (ie. MSHFS1NTR-RoHS) for Tape & Reel and RoHS Compliant version.

Digital Levels

All the clock and control pins (except FSEL, CLK and G) are referenced between GND and VDD. In single supply applications, the digital levels should be CMOS levels from VSS to VDD. In dual supply systems, the digital levels should be CMOS levels from GND to VDD.

Input Selection

The input is selected using the Input Select Pins S1 and S2.

S2	S1	Input
0	0	1
0	1	2
1	0	3
1	1	4

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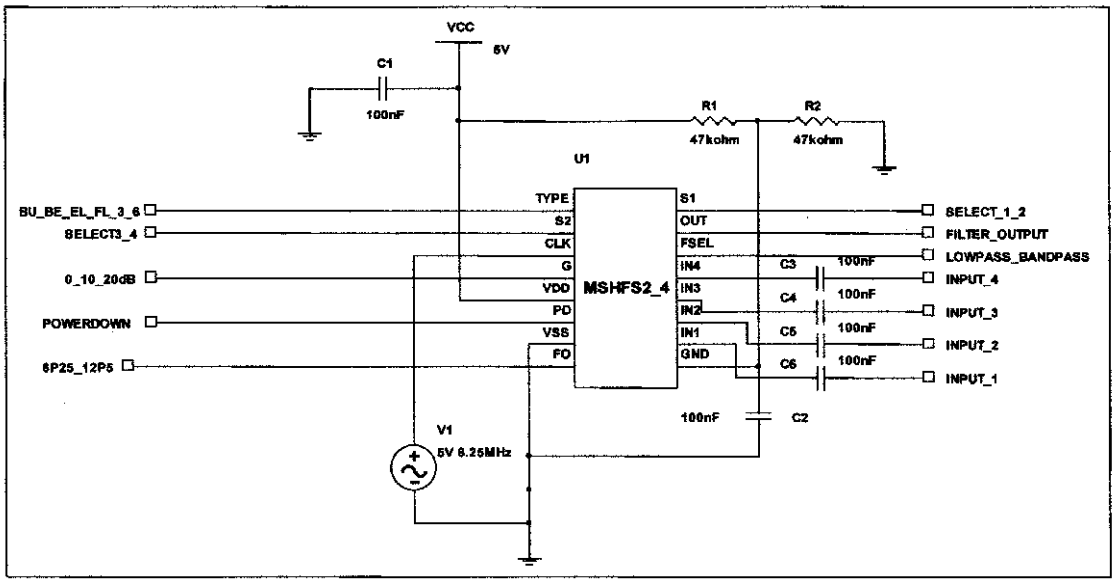
Application Schematics

Mux part - Single supply operation



Single part - Single supply operation