



# Total Harmonic Distortion Analyzer

## Data Sheet

### Description

The MSTHDA is a single chip 1/6<sup>th</sup> octave-wide 5 harmonic Total Harmonic Distortion analyzer whose center frequencies are controlled by a single master clock. The center frequencies are set at the fundamental, second harmonic, third harmonic, fourth harmonic and fifth harmonic frequency. The sample to corner is 25:1 for the fifth-harmonic output and 125:1 at the fundamental output (Double Sampled). The fifth harmonic output is 3.4 MHz when clocked at 42.5 MHz (MSTHDA-1).

The MSTHDA includes two uncommitted op amps for adding additional fixed gain for microphone or other low level applications. A digitally programmable gain stage provides 0, 10 or 20 dB of gain. The PD pin selects power down, low power for ultrasonic applications and regular power for high frequency operation.

The MSTHDA is fabricated in 0.6 um CMOS process for low power consumption and operation from 3.0 to 5.5 VDC. All packages are 150 mil wide (Narrow SOIC)

### Features

- Selectable Power Modes as low as 2 mA (3V)
- Power Down Mode to 400 uA
- Operates from 3.0 V to 5.5 VDC
- 5 6 pole Bandpass filters in one package
- Digitally controlled gain stage
- Two Uncommitted Op Amps
- No Microprocessor Needed

### Applications

- Multi-standard RFID Readers (MSTHDA-1)
- Real-Time Distortion Analysis
- Audio and Ultrasonic Analysis
- Vibration Analysis

### Ordering Information

Part Number	Package	Operating Temperature
MSTHDAN	SOIC-16N	-40 <sup>o</sup> to +85 <sup>o</sup> C

### Absolute Maximum Ratings

Power Supply Voltage	+6V
Storage Temperature Range	-60 to +150 <sup>o</sup> C
Operating Temperature Range	-40 to +85 <sup>o</sup> C

MSTHDA

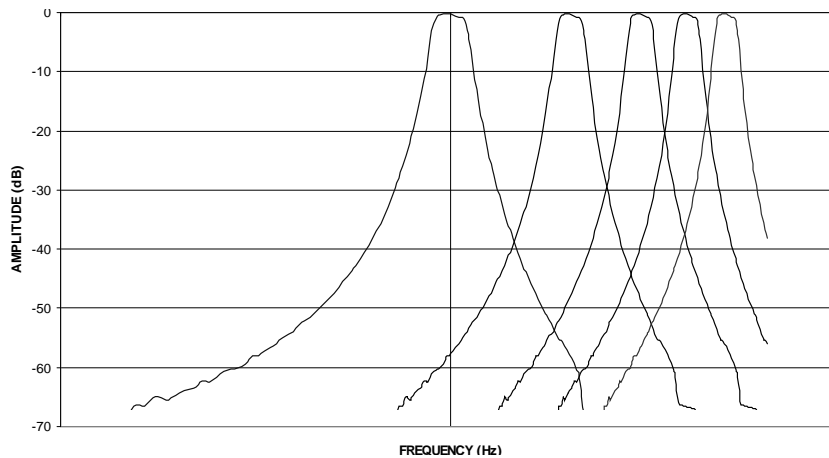


Figure 1: Normalized Frequency Response





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## Electrical Characteristics \_\_\_\_\_

(VDD = +5.0V, T = 25 C)

MSTHDA

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DC Specifications</b>						
Operating Voltage	VDD		3.3	5.0	5.5	V
Supply Current	IDD	PD=VDD RBias=100k		110		mA
Supply Current	IDD	PD=VDD		15		mA
Supply Current	IDD	PD=VDD/2		5		mA
Powerdown Current	IDD <sub>PD</sub>	PD=VSS		400		μA
Input Impedance	RI			10		MΩ
Output Impedance	RO			500		Ω
Supply Current	IDD	PD=1/2*VDD VDD=3.3V	0.5	1.0	2.0	mA
<b>AC Specifications</b>						
-40 dB Bandwidth			0.76		1.32	Hz/Hz
Maximum Center Frequency		Output 5 PD=VDD/2V		1		MHz
Maximum Center Frequency		Output 5 PD=5V		2		MHz
Bandpass Q	Q			9.0		
Output Capacitive Load					20	pF
Output Signal Swing		RL = 10 MΩ		4.0		V <sub>pp</sub>
Noise	e <sub>n</sub>	To 1/2 Sample		180		μVrms
Clock to Corner Filter 1		Sample Rate is 2x Clock		62.5		Hz/Hz
Clock to Corner Filter 2		Sample Rate is 2x Clock		31.25		Hz/Hz
Clock to Corner Filter 3		Sample Rate is 2x Clock		20.83		Hz/Hz
Clock to Corner Filter 4		Sample Rate is 2x Clock		15.625		Hz/Hz
Clock to Corner Filter 5		Sample rate is 2x Clock		12.5		Hz/Hz
Gain	A <sub>V</sub>		-0.5	0.0	0.5	dB
Output Offset Voltage	VOS	V <sub>IN</sub> = 1 Vrms		50		mV
Distortion	THD			-71		dB





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## Block Diagram

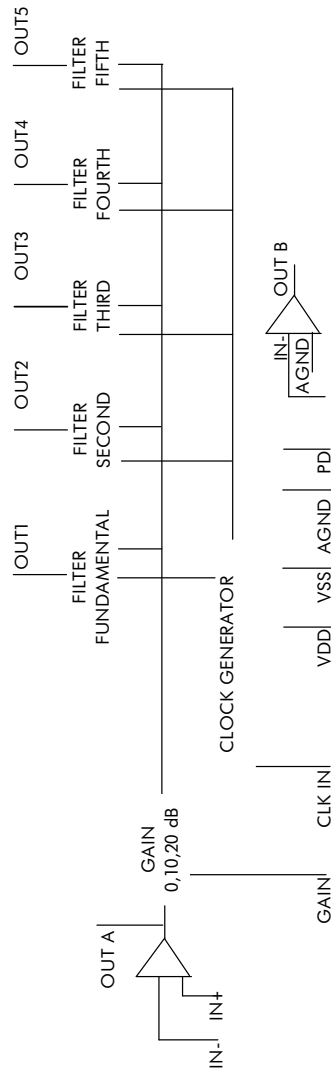


Figure 2: Msthda BLOCK DIAGRAM

MSTHDA

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# Total Harmonic Distortion Analyzer Data Sheet

## Pin Description

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- |         |   |          |   |
|---------|---|----------|---|
| 1. INB  | Inverting Uncommitted Op Amp Input B                      | 9. PD    | Power Down; When CMOS high, device is powered down. |
| 2. OUTA | Op Amp Output A   | 10. OUT1 | Fundamental Filter Output                           |
| 3. INA  | Inverting Op Amp Input A                                  | 11. OUT2 | Second Harmonic Filter Output                       |
| 4. BIAS | Bias Input on MSTHD-1                                     | 12. OUT3 | Third Harmonic Filter Output                        |
| IPA     | Noninverting Op Amp Input A MSTHD                         | 13. OUT4 | Fourth Harmonic Filter Output                       |
| 5. AGND | Connect to 1/2 VDD  | 14. OUT5 | Fifth Harmonic Filter Output                        |
| 6. CLK  | CMOS Clock adjusts position of bandpass filter outputs.   | 15. VDD  | Positive Supply Typically 5.0 VDC                   |
| 7. VSS  | Negative Supply; Tie to OVDC                              | 16. OUTB | Uncommitted Op Amp B Output.                        |
| 8. GAIN | Tertiary Control: 0V, 0 dB,<br>1/2 VDD 10 dB<br>VDD 20 dB |          |   |

INB	1	16	OUTB
OUTA	2	15	VDD
INA	3	14	OUT5
BIAS/IPA	4	13	OUT4
AGND	5	12	OUT3
CLK	6	11	OUT2
VSS	7	10	OUT1
GAIN	8	9	PD

Figure 3: MSTHDA/MSTHDA-1 Pinout





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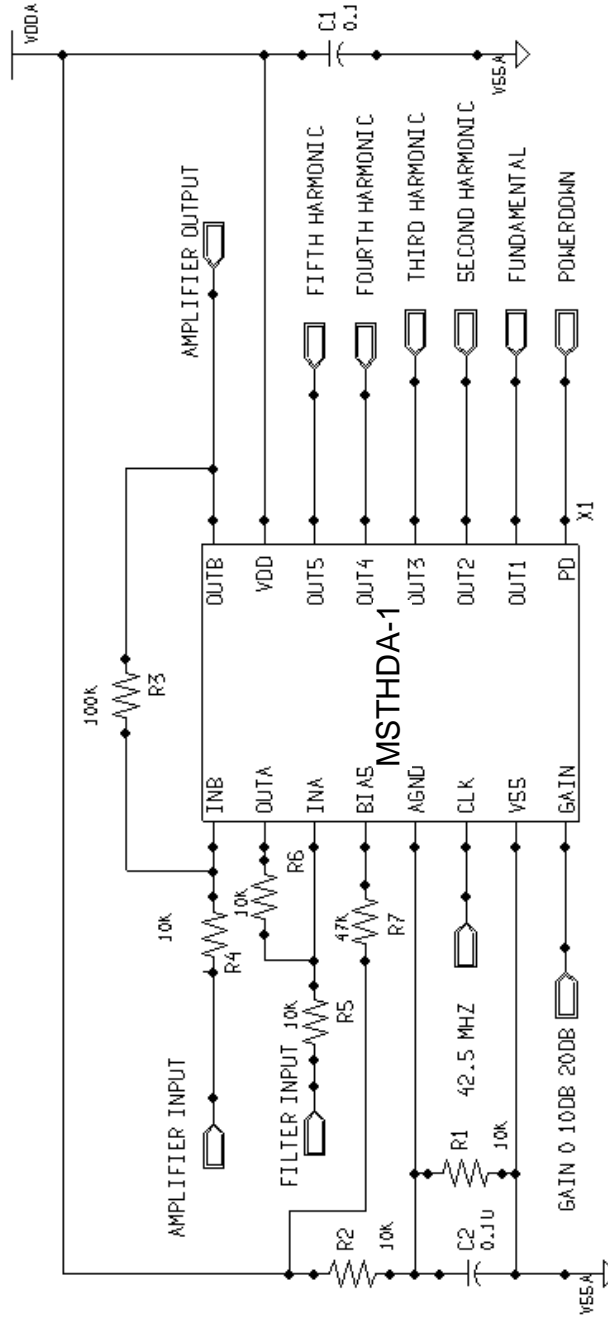


Figure 4: MSTHDA-1 Application Schematic (RFID Reader)

MSTHDA





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## MSTHDA

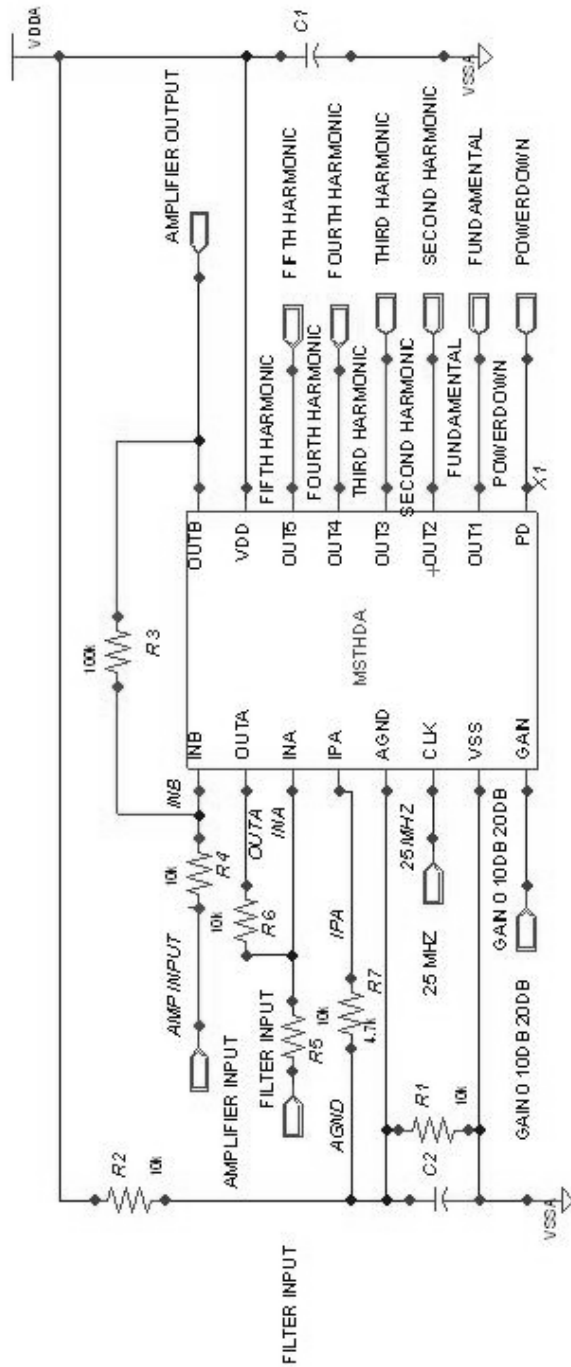


Figure 5: MSTHDA Application Schematic






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 STANDARD PRODUCTS
 

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MSGEQ5A/MSGEQ7	Five Band/Seven Band Graphic Equalizer
MSVHFS1-6	Selectable Very High Frequency LP/BP Filter
MSHFS1-6	Selectable High Frequency LP/BP Filter
MSFS1-6	Selectable Lowpass/Bandpass Filter
MSU1F1-4, MSU2F1	Resistor Programmable Universal Active Filter
MSU1HF1-4, MSU2HF1	High Frequency Resistor Programmable Universal Active Filter
MSELP	Switched Capacitor Elliptic Lowpass Filter with Op Amps
MSNBLP	Switched Capacitor Butterworth Lowpass Filter
MSLE/B/C5L/M	Switched Capacitor General Purpose Lowpass Filter
MS2LFS	Dual Selectable Low Voltage Lowpass/Bandpass Filter
MSLFS	Selectable Low Voltage Lowpass/Bandpass Filter
MSHN1-6	Selectable High Pass/Notch Filter
MSRAAF	Resistor Programmable Active Audio Filter
MSRAHF	Resistor Programmable Active High Frequency Filter
MSDET	Tone Detector
MSEPAF	Electrically Programmable Active Filter
MSCBT	Communications Baseband Transceiver
MSLV14	14 MHz Video Lowpass Filter
MSSPSI	Smart Programmable Sensor Interface
MSCPSI	Computer Programmable Sensor Interface
MSTHDA	Total Harmonic Distortion Analyzer
MSSCSA	Single Chip Spectrum Analyzer
MSFIPS	FIP-140 Level 4+ Security Supervisor
MSLSA	Low Power Single Chip Spectrum Analyzer
MSRFIF	Radio Frequency Interface Front-End

MSTHDA





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